AMENDMENTS TO THE CLAIMS

Please amend claims 1 and 10, as set forth in the listing of claims that follows, which will replace all prior versions and listings, of claims in the application:

**Listing of Claims**

1. (Currently Amended) A circuit board assembly comprising:

a co-fired substrate comprising at least first and second regions superimposed and bonded to each other, the first region being formed of a plurality of superimposed first ceramic layers, each first ceramic layer consisting essentially of low thermal conductivity, electrically-nonconductive materials, at least some of the first ceramic layers being bonded to each other, and the second region being formed of at least one second ceramic layer containing thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive materials, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive materials of the first and second ceramic layers;

conductor lines on at least some of the first ceramic layers so as to be between adjacent pairs of the first ceramic layers;

electrically-conductive vias that extend through at least some of the first ceramic layers and electrically interconnect the conductor lines on the first ceramic layers; and

a surface-mount IC device mounted to a first surface of the substrate defined by one of the low thermal conductivity first ceramic layers, wherein said first and second regions are arranged for serial thermal interconnection between said IC device and an opposed heat sink, and wherein each first ceramic layer and said at least one second ceramic layer have substantially similar width and length characteristic dimensions.

2. (Original) A circuit board assembly according to claim 1, wherein the substrate is a low-temperature co-fired ceramic substrate.

3. (Original) A circuit board assembly according to claim 1, wherein the thermally-conductive particles are metal and/or ceramic particles.

4. (Original) A circuit board assembly according to claim 1, wherein the substrate does not contain any thermal vias extending through the substrate from the surface-mount device on the first surface to an oppositely-disposed second surface of the substrate.

5. (Withdrawn) A circuit board assembly according to claim 1, wherein the substrate contains thermal vias that extend from the surface-mount device on the first surface to but not into the second region of the substrate.

6. (Original) A circuit board assembly according to claim 1, wherein the second ceramic layers have a coefficient of thermal expansion of within about 4 ppm/°C of first ceramic layers.

7. (Original) A circuit board assembly according to claim 1, wherein the second ceramic layers have a thermal conductivity of at least 10 W/mK.

8. (Original) A circuit board assembly according to claim 1, wherein the second ceramic layer is one of a plurality of second ceramic layers bonded surface-to-surface to form the second region of the substrate, the second region is free of the first ceramic layers, the first ceramic layers are bonded surface-to-surface to form the first region of the substrate, and the first region is free of the second ceramic layers and is bonded to the second region of the substrate.

9. (Original) A circuit board assembly according to claim 1, further comprising a heat sink bonded to the substrate, the second region of the substrate being between the heat sink and the first region of the substrate.

10. (Currently Amended) A circuit board assembly comprising:

a low-temperature co-fired substrate comprising first and second regions superimposed and bonded to each other, the first region being formed of a plurality of superimposed first ceramic layers that are bonded to each other, each first ceramic layer consisting essentially of low thermal conductivity electrically-nonconductive glass and ceramic materials, and the second region being formed of second ceramic layers that are superimposed, bonded to each other, and contain thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive glass and ceramic materials, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive glass and ceramic materials of the first and second ceramic layers, the first region of the substrate being free of the second ceramic layers and the second region of the substrate being free of the first ceramic layers and being bonded to the first region of the substrate, the second ceramic layers having thermal conductivities of at least 10 W/mK and having coefficients of thermal expansion of within about 4 ppm/°C of the first ceramic layers;

conductor lines on at least some of the first ceramic layers so as to be between adjacent pairs of the first ceramic layers;

electrically-conductive vias that electrically interconnect the conductor lines on different first ceramic layers; and

a surface-mount IC device mounted to a first surface of the substrate defined by one of the low thermal conductivity, first ceramic layers;

wherein the substrate does not contain any thermal vias extending through the second region or the second ceramic layers, wherein said first and second regions are arranged for serial thermal interconnection between said IC device and an opposed heat sink, and wherein each first ceramic layer and said at least one second ceramic layer have substantially similar width and length characteristic dimensions.

11. (Withdrawn) A process of forming a circuit board assembly, the process comprising the steps of:

providing green tapes of which at least a first plurality thereof consist essentially of electrically-nonconductive materials in a binder and of which at least a second green tape thereof contains thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive materials and a binder, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive materials of the green tapes;

forming vias through at least some of the first plurality of the green tapes;

depositing an electrically-conductive material within the vias and depositing an electrically-conductive material on surfaces of the first plurality of the green tapes;

collating and laminating the green tapes together to form a green substrate;

co-firing the green substrate to form a co-fired substrate comprising at least first and second regions superimposed and bonded to each other, the first region comprising first ceramic layers that are superimposed and formed by the first plurality of the green tapes, the second region comprising a second ceramic layer formed by the second green tape, at least some of the first ceramic layers of the first region being bonded to each other, the electrically-conductive material on the surfaces of the first plurality of the green tapes forming conductor lines between adjacent pairs of the first ceramic layers, the vias filled with the electrically-conductive material forming electrically-conductive vias that electrically interconnect the conductor lines on the first ceramic layers; and then

mounting a surface-mount IC device to a first surface of the substrate defined by one of the first ceramic layers.

12. (Withdrawn) A process according to claim 11, wherein the green substrate is co-fired at a temperature of about 900°C.

13. (Withdrawn) A process according to claim 11, wherein the thermally-conductive particles are metal and/or ceramic particles.

14. (Withdrawn) A process according to claim 11 wherein, as a result of the collating, laminating and co-firing steps, the substrate does not contain any thermal vias extending through the substrate from the surface-mount device on the first surface to an oppositely-disposed second surface of the substrate.

15. (Withdrawn) A process according to claim 11, further comprising steps of:

forming second vias through the first plurality of the green tapes; and

depositing a thermally-conductive material within the second vias;

wherein as a result of the collating and laminating step the second vias are aligned and as a result of the co-firing step the substrate contains thermal vias that extend from the surface-mount device on the first surface to but not into the second region of the substrate.

16. (Withdrawn) A process according to claim 11, wherein the second ceramic layer has a thermal conductivity of at least 10 W/mK.

17. (Withdrawn) A process according to claim 11, wherein the second ceramic layer has a coefficient of thermal expansion of within about 4 ppm/°C of the first ceramic layers.

18. (Withdrawn) A process according to claim 11 wherein the green tapes comprise a plurality of second green tapes containing thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive materials and a binder

19. (Withdrawn) A process according to claim 18 wherein, as a result of the collating, laminating and co-firing steps, the second green tapes form second ceramic layers that are bonded surface-to-surface to form the second region of the substrate, the second region is free of the first ceramic layers, the first ceramic layers are bonded surface-to-surface to form the first region of the substrate, and the first region is free of the second ceramic layers.

20. (Withdrawn) A process of forming a circuit board assembly, the process comprising:

providing a plurality of green tapes, at least a first plurality of the green tapes consisting essentially of electrically-nonconductive glass and ceramic materials in a binder, at least a second plurality of the green tapes containing thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive glass and ceramic materials and a binder, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive materials of the first and second pluralities of green tapes;

forming vias through at least some of the first plurality of green tapes but not through any of the second plurality of green tapes;

depositing an electrically-conductive material within the vias and depositing an electrically-conductive material on surfaces of the first plurality of green tapes;

collating and laminating the plurality of green tapes together to form a green substrate in which the first plurality of green tapes are collated and laminated to be surface-to-surface to form a first region of the green substrate that is free of the second plurality of the green tapes and the second plurality of the green tapes are collated and laminated to be surface-to-surface to form a second region of the green substrate that is free of the first plurality of the green tapes;

co-firing the green substrate at a temperature of about 900°C to form a co-fired substrate comprising first and second regions superimposed and bonded to each

other, the first region being formed by the first region of the green substrate so as to contain first ceramic layers that are superimposed, bonded to each, and formed by the first plurality of the green tapes, the second region being formed by the second region of the green substrate so as to contain second ceramic layers that are superimposed, bonded to each, and formed by the second plurality of the green tapes, the electrically-conductive material on the surfaces of the first plurality of the green tapes forming conductor lines between adjacent pairs of the first ceramic layers, the vias filled with the electrically-conductive material forming electrically-conductive vias that electrically interconnect the conductor lines on adjacent pairs of the first ceramic layers, the second ceramic layers having thermal conductivities of at least 10 W/mK and having coefficients of thermal expansion of within about 4 ppm/°C of the first ceramic layers; and then

mounting a surface-mount IC device to a first surface of the substrate defined by one of the first ceramic layers;

wherein the substrate does not contain any thermal vias extending through the second region or the second ceramic layers.